

What is claimed is:

1. A semiconductor memory comprising:
a first conductivity type semiconductor substrate and
one or more memory cells constituted of an island-like
5 semiconductor layer, a charge storage layer and a control gate,
the charge storage layer and the control gate being formed to
entirely or partially encircle a sidewall of the island-like
semiconductor layer,
wherein at least one of said one or more memory cells
10 is electrically insulated from the semiconductor substrate.
2. A semiconductor memory according to claim 1,
wherein said at least one memory cell is electrically insulated
from the semiconductor substrate by a second conductivity
type impurity diffusion layer formed in the semiconductor
15 substrate or in the island-like semiconductor layer, or by a
second conductivity type impurity diffusion layer and a first
conductivity type impurity diffusion layer formed in the second
conductivity type impurity diffusion layer.
3. A semiconductor memory according to claim 1,
20 wherein a plurality of memory cells are formed with
regard to one island-like semiconductor layer and
at least one of the memory cells is electrically
insulated from another memory cell by a second conductivity
type impurity diffusion layer formed in the island-like
25 semiconductor layer, or by a second conductivity type impurity
diffusion layer and a first conductivity type impurity diffusion
layer formed in the second conductivity type impurity diffusion
layer.

4. A semiconductor memory according to claim 1,
wherein the memory cell is electrically insulated from
the semiconductor substrate by
a second conductivity type impurity diffusion layer
5 formed in the semiconductor substrate or in the island-like
semiconductor layer and
a depletion layer formed at a junction between the
second conductivity type impurity diffusion layer and the
semiconductor substrate or the island-like semiconductor
10 layer.
5. A semiconductor memory according to claim 1,
wherein a plurality of memory cells are formed with
regard to one island-like semiconductor layer and
at least one of the memory cells is electrically
15 insulated from another memory cell by a second conductivity
type impurity diffusion layer formed in the semiconductor
substrate or the island-like semiconductor layer and a
depletion layer formed at a junction between the second
conductivity type impurity diffusion layer and the
20 semiconductor substrate or the island-like semiconductor
layer.
6. A semiconductor memory according to claim 1,
wherein a second conductivity type impurity diffusion layer
formed in the semiconductor substrate functions as common
25 wiring for at least one memory cell.
7. A semiconductor memory according to claim 1,
wherein a plurality of memory cells are formed with regard to
one island-like semiconductor layer and the memory cells are

arranged in series.

8. A semiconductor memory according to claim 1,
wherein a plurality of island-like semiconductor layers
are formed in matrix,

5 impurity diffusion layers for reading a state of a
charge stored in a memory cell are formed in the island-like
semiconductor layers,

a plurality of control gates are provided continuously
in a direction to form a control gate line and

10 a plurality of the impurity diffusion layers in a
direction crossing the control gate line are connected to form a
bit line.

9. A semiconductor memory according to claim 1,
wherein a gate electrode for selecting a memory cell is formed
15 at least at an end of the memory cell formed on the island-like
semiconductor layer so as to partially or entirely encircle the
sidewall of the island-like semiconductor layer and the gate
electrode is arranged in series with the memory cell.

10. A semiconductor memory according to claim 9,
20 wherein a part of the island-like semiconductor layer opposed
to the gate electrode is electrically insulated from the
semiconductor substrate or the memory cell by a second
conductivity type impurity diffusion layer formed on the
semiconductor substrate or in the island-like semiconductor
25 layer.

11. A semiconductor memory according to claim 1,
wherein a plurality of memory cells are formed with regard to
one island-like semiconductor layer and control gates

constituting the memory cell are arranged so closely that
channel layers of memory cells are electrically connected.

12. A semiconductor memory according to claim 9 or 10,
wherein the control gate and the gate electrode are disposed so
5 closely that a channel layer located in a part of the island-like
semiconductor layer opposed to the gate electrode is
electrically connected to a channel layer of the memory cell.

13. A semiconductor memory according to claim 1,
wherein a plurality of memory cells are formed with regard to
10 one island-like semiconductor layer, and an electrode for
electrically connecting channel layers of memory cells is further
formed between control gates.

14. A semiconductor memory according to claim 9 or 10,
wherein a plurality of memory cells are formed with regard to
15 one island-like semiconductor layer, and an electrode for
electrically connecting a channel layer located in a part of the
island-like semiconductor layer opposed to the gate electrode
to a channel layer of the memory cell is further formed between
the control gate and the gate electrode.

15. A semiconductor memory according to claim 9, 10, 12
or 14, wherein all, some or one control gate(s) are formed of
the same material as all, some or one gate electrode(s).

16. A semiconductor memory according to claim 9, 10, 12
or 14, wherein the charge storage layer and the gate electrode
25 are formed of the same material.

17. A semiconductor memory according to claim 1,
wherein a plurality of island-like semiconductor layers are
formed in matrix, and the width of the island-like

semiconductor layers in one direction is smaller than a distance between adjacent island-like semiconductor layers in the same direction.

18. A semiconductor memory according to claim 1,
5 wherein a plurality of island-like semiconductor layers are formed in matrix, and a distance between the island-like semiconductor layers in one direction is smaller than a distance between the island-like semiconductor layers in another direction.

- 10 19. A semiconductor memory according to claim 1,
wherein a lower gate electrode, the control gate and/or an upper gate electrode are arranged in an upward order in a direction vertical to the semiconductor substrate,
and
15 the upper gate electrode, the control gate and/or the lower gate electrode are sequentially led out to a surface of the semiconductor memory at an end of a memory cell array in which island-like semiconductor layers with the memory cells formed thereon are arranged in matrix.

- 20 20. A process for producing a semiconductor memory having at least one memory cell constituted of an island-like semiconductor layer, a charge storage layer and a control gate, the charge storage layer and the control gate being formed to entirely or partially encircle a sidewall of the island-like
25 semiconductor layer, the process comprising the steps of:
forming at least one island-like semiconductor layer on a semiconductor substrate;
forming an insulating film and a first conductive film

over a surface of the island-like semiconductor layer;

forming sidewall spacers of an insulating film separated in a vertical direction on the first conductive film located on a sidewall of the island-like semiconductor layer;

5 separating the first conductive film using the sidewall spacers as a mask;

introducing an impurity in self-alignment with respect to the separated first conductive films; and

forming an interlayer insulating film and a second
10 conductive film on the first conductive films.

21. A process for producing a semiconductor memory having at least one memory cell constituted of an island-like semiconductor layer, a charge storage layer and a control gate, the charge storage layer and the control gate being formed to
15 entirely or partially encircle a sidewall of the island-like semiconductor layer, the process comprising the steps of:

forming at least one island-like semiconductor layer on a semiconductor substrate;

forming a charge storage layer of a laminated
20 insulating film and a first conductive film over a surface of the island-like semiconductor layer;

forming sidewall spacers of an insulating film separated in a vertical direction on the first conductive film located on a sidewall of the island-like semiconductor layer;

25 separating the first conductive film using the sidewall spacers as a mask; and

introducing an impurity in self-alignment with respect to the separated first conductive films.

22. A process for producing a semiconductor memory having at least one memory cell constituted of an island-like semiconductor layer, a charge storage layer and a control gate, the charge storage layer and the control gate being formed to
5 entirely or partially encircle a sidewall of the island-like semiconductor layer, the process comprising the steps of:

forming at least one island-like semiconductor layer on a semiconductor substrate;
introducing an impurity partially in the island-like
10 semiconductor layer;
forming an insulating film and a first conductive film over a surface of the island-like semiconductor layer;
forming sidewall spacers of an insulating film separated in a vertical direction on the first conductive film
15 located on a sidewall of the island-like semiconductor layer;
and
separating the first conductive film using the sidewall spacers as a mask.

23. A process according to any one of claims 20 to 22,
20 wherein the introduced impurity is diffused so that a continuous impurity diffusion layer is formed in the island-like semiconductor layer in a direction horizontal to a surface of the semiconductor substrate.

24. A process according to any one of claims 20 to 22,
25 wherein a plurality of island-like semiconductor layers are formed in matrix, sidewalls of the island-like semiconductor layers are oxidized to form oxide films, and the oxide films are removed so that the width of the island-like semiconductor

layers in one direction is smaller than a distance between the island-like semiconductor layers in the same direction.

25. A process according to any one of claims 20 to 22, wherein a third conductive film is formed between separated
5 first conductive films.

26. A process according to any one of claims 20 to 22, wherein the first conductive film is separated into two or more separated first conductive films which are located so closely that a channel layer formed beneath a separated first
10 conductive film along the island-like semiconductor layer is electrically connected to an adjacent channel layer.

27. A process according to claim 20 or 22, wherein an insulating film is formed in a part of a surface of the island-like semiconductor layer, another insulating film is
15 formed in another part of the surface of the island-like semiconductor layer, and the first conductive film is formed on the insulating film and on said another insulating film.

28. A process according to claim 21, wherein the charge storage layer of the laminated insulating film is formed in a
20 part of a surface of the island-like semiconductor layer, another insulating film is formed in another part of the surface of the island-like semiconductor layer, and the first conductive film is formed on the charge storage layer and on said another insulating film.

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